Freescale Semiconductor
Product Brief

Document Number: MC9328MX21P
Rev. 2.1, 07/2007

MC9328MX21 Applications Processor

Freescale's i.MX family of microprocessors has demonstrated leadership in the portable handheld market. Building on the success of the MX (Media Extensions) series, the i.MX21 (MC9328MX21) provides a leap in performance with an ARM926EJ-S™ microprocessor core that provides accelerated Java support in addition to highly integrated system functions.The i.MX21 device specifically addresses the needs of the smartphone and portable product markets with intelligent integrated peripherals, advanced processor core, and power management capabilities.

The i.MX21 features the advanced and power-efficient ARM926EJ-S core operating at speeds up to 266 MHz and is part of a growing family of *Smart Speed* products that offer high performance processing optimized for lowest power consumption. On-chip modules such as a video accelerator module, LCD controller, USB On-The-Go, 1-Wire® interface, CMOS sensor interface, and synchronous serial interfaces offer designers a rich suite of peripherals that can enhance many products seeking to provide a rich multimedia experience.

For cost sensitive applications, the NAND Flash controller allows the use of low cost Nand Flash devices

Contents

to be used as primary or secondary non-volatile storage. The on-chip ECC and parity checking circuitry of the Nand Flash controller frees the CPU for other tasks. WLAN, Bluetooth and expansion options are provided through PCMCIA/CF, USB, and MMC/SD host controllers.

The i.MX21 processor is packaged in a 289-pin molded array process ball grid array (MAPBGA).

A summary of the main features of the i.MX21 processor includes:

- High level of on-chip integration
- Very low-power system design without compromised performance
- Optimized for multimedia applications
- Optimized for Bluetooth applications with high-speed interfaces to external Bluetooth solutions
- Dedicated graphics accelerator port
- Supports a wide variety of applications including the most popular smartphones, PDAs, and next-generation wireless communicators

1 i.MX21 Block Diagram

Figure 1 is a simplified functional block diagram of the i.MX21 processor.

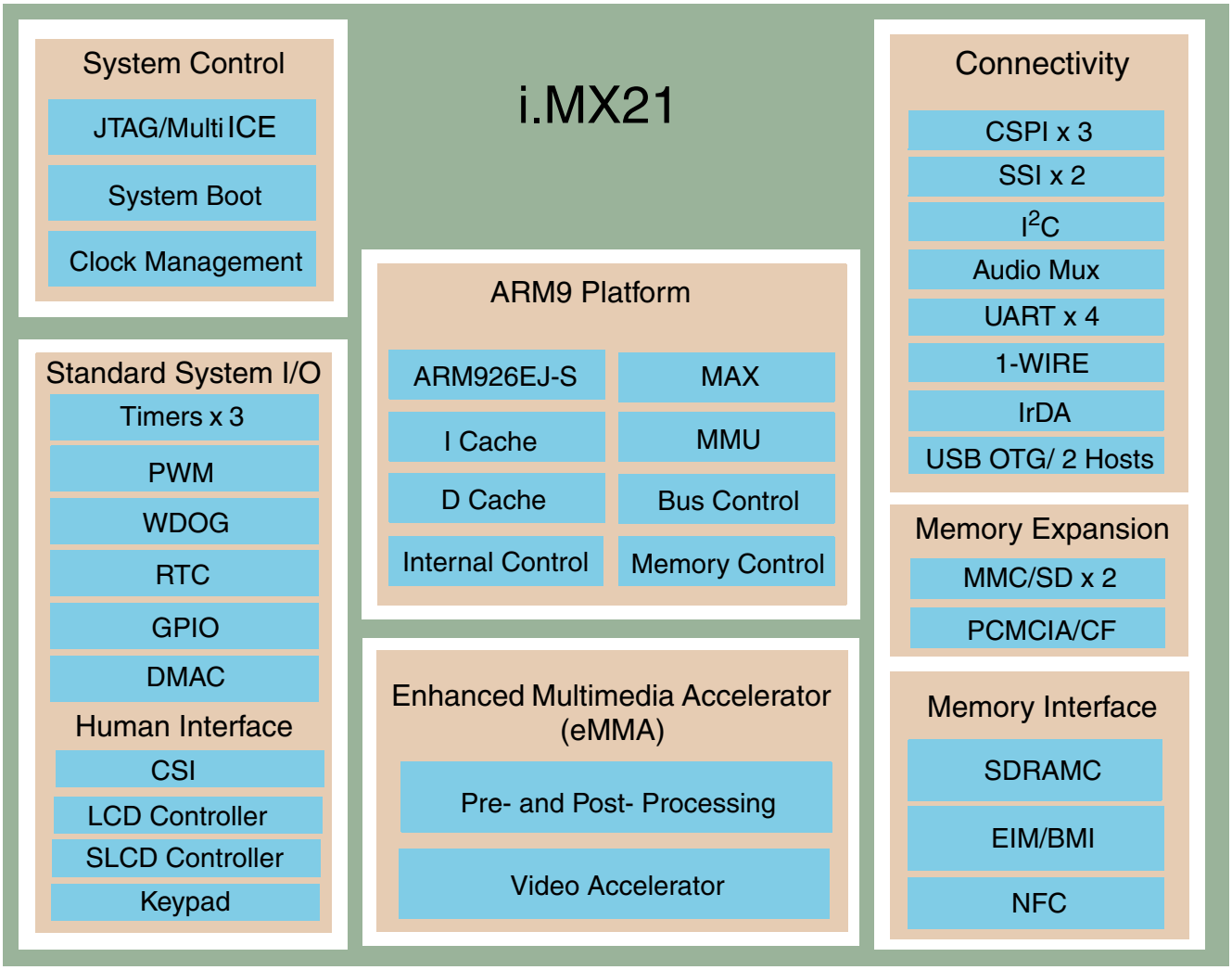

Figure 1. i.MX21 Functional Block Diagram

2 i.MX21 Features

The MC9328MX21 boasts a robust array of features that can support a wide variety of applications. This section provides a brief description of these features.

2.1 ARM926EJ-S Core Complex

The ARM926EJ-S Core Complex (also known as the ARM926 Platform) consists of the ARM926EJ-S processor, a 6 × 4 Multi-Layer AHB crossbar switch, and a primary AHB complex.

- ARM926EJ-S microprocessor core
  - 16K instruction cache and 16K data cache

- High-performance ARM® 32-bit RISC engine
- Thumb® 16-bit compressed instruction set for a leading level of code density
- Efficient execution of Java byte codes
- EmbeddedICE™ JTAG software debug
- 100 percent user code binary compatibility with ARM7TDMI™
- Advanced Microcontroller Bus Architecture (AMBA™) system-on-chip multi-master bus interface
- Support for mixed loads of real-time and user applications via cache locking facilities
- Virtual Memory Management Unit (VMMU)

- ARM Interrupt Controller (AITC)
  - The AITC is connected to the primary AHB as a slave device and provides support for up to 64 interrupt sources. It generates normal and fast interrupts to the processor core. The AITC supports a hardware assisted vectoring mode for automatic vectoring to reduce interrupt latency.
- Digital Phase-Locked Loops (DPLLs) and Power Control Module
  - Digital phase-locked loops (DPLLs) and clock controller for all internal clock generation
  - MCUPLL generates system and CPU clocks from a 26MHz crystal
  - USBPLL generates 48 MHz clock for the USB OTG from either a 26 MHz crystal or 32kHz
  - Support for three power modes for different power consumption needs: run, doze, and stop.
- AHB to IP bus interfaces (AIPIs)
  - Provide a communication interface between the high-speed AHB to a lower-speed IP bus for slave peripherals
- The Multi-Layer 6 × 4 AHB Crossbar Switch
  - The crossbar switch allows for concurrent transactions to proceed from any input port (bus master) to any output port (bus slave). That is, it is possible for all four output ports to be active at the same time as a result of four independent input or output requests.
- CPU and System speed
  - ARM926EJ-S core: up to 266 MHz
  - System Clock: up to 133 MHz
  - External memory interface: same clock source as system, up to 133 MHz at 1.8V supply
  - System clock is derived from the CPU clock through an integer divider

2.2 System Control and Timers

The i.MX21 processor contains various timers and system control features to optimize the control of both the internal modules and external devices.

2.2.1 Watchdog Timer

The Watchdog Timer module (WDOG Timer) provides the following:

- Programmable time out of 0.5 s to 64 s
- Resolution of 0.5 s

2.2.2 Real-Time Clock/Sampling Timer

The Real-Time Clock (RTC) module maintains the system clock, provides stopwatch, alarm, and interrupt functions, and supports the following features:

- 32.768 kHz and 32 kHz input operation
- Full clock features: seconds, minutes, hours, days
- Capable of counting up to 512 days
- Minute countdown timer with interrupt
- Programmable daily alarm with interrupt
- Sampling timer with interrupt
- Once-per-second, once-per-minute, once-per-hour, and once-per-day interrupts
- Interrupt generation for digitizer sampling or keyboard debouncing

2.2.3 Three General-Purpose 32-Bit Counters/Timers

The General-Purpose Timer (GPT) module contains three identical general-purpose 32-bit timers with programmable prescalers and compare and capture registers with the following features:

- Automatic interrupt generation
- Programmable timer input/output pins
- Input capture capability with programmable trigger edge
- Output compare with programmable mode

2.2.4 Pulse-Width Modulator Module

The following features characterize the Pulse-Width Modulator (PWM) module:

- 4×16 FIFO to minimize interrupt overhead
- 16-bit resolution
- Sound and melody generation

2.2.5 General-Purpose I/O Ports

The GPIO module provides six general purpose I/O ports. Each single GPIO port is a 32-bit port that may be multiplexed with one or more dedicated functions. The GPIO features are:

- Supports level or edge trigger interrupt and is system wake-up capable
- Most I/O signals are multiplexed with dedicated functions for pin efficiency

2.2.6 Endianness

The i.MX21 processor system supports little endian only.

2.3 Memory Interface

The memory interfaces of the i.MX21 processor consist of the SDRAM controller, the Direct Memory Access controller, the NAND Flash controller and the External Interface module. The individual features of these controllers are provided in this section.

2.3.1 SDRAM Controller

The SDRAM controller (SDRAMC) consists of 7 major blocks, including the SDRAM command controller, page and bank address comparators, row/column address multiplexer, data aligner/multiplexer, configuration registers, refresh request counter, and the powerdown timer.

The features offered by the SDRAMC are as follows:

- Support for four banks of single data rate 64 Mbit, 128 Mbit, and 256 Mbit SDRAM
  - — Two independent chip-selects with up to 64 Mbyte per chip-select
  - — Up to four banks active simultaneously for each chip-select
  - — JEDEC standard pinout and operation
  - — Boot capability from CSD1
- PC133-compliant interface
  - — 133 MHz system clock achievable with “-8” option PC133-compliant memories
  - — Single and fixed-length (4-word) burst access
  - — Access time of 8-1-1-1 at 133 MHz
- Software configurable for differing system requirements
  - — 16-bit or 32-bit bus width
  - — Configurable row cycle delay (tRC), row precharge delay (tRP), row-to-column delay (tRCD), and column-to-data delay (CAS latency)
- Built-in auto-refresh timer and state machine
- Hardware-supported self-refresh entry and exit: capability to maintain valid data during system reset and low-power modes
- Auto-powerdown (clock suspend) timer

2.3.2 Direct Memory Access Controller

The Direct Memory Access Controller (DMAC) provides 16 channels to support linear memory, 2D memory, FIFO and end-of-burst enable FIFO transfers to support a wide variety of DMA operations. Features include:

- Supports 16 channels linear memory, 2D memory and FIFO for both source and destination
- Supports 8-bit, 16-bit, or 32-bit FIFO port size and memory port size data transfer
- DMA burst length is configurable up to maximum of 16 words, 32 half-words, or 64 bytes for each channel

- Bus utilization control for a channel that is not triggered by DMA request
- Interrupts provided to interrupt handler on bulk data transfer complete or transfer error
- DMA burst time-out error to terminate DMA cycle when the burst cannot be completed in a programmed timing period
- Dedicated external DMA request and grant signal
- Support increment, decrement and no increment for source and destination addressing
- Supports DMA chaining

2.3.3 NAND Flash Controller

The NAND Flash controller (NFC) interfaces standard NAND Flash parts to the i.MX21 processor and hides the complexities of accessing NAND Flash. The NFC features include:

- Contains hardware bootloader for automatic boot up from NAND Flash devices
- Supports all 8-bit/16-bit NAND Flash devices regardless of density and organization
- Supports 512 byte and 2 Kbyte page sizes
- Internal 2 Kbyte of buffer RAM used as boot RAM during cold startup and as read/write page buffers to relieve CPU intervention
- Automatic ECC detection and selectable correction
- Data protection for ram buffer and NAND Flash pages

2.3.4 External Interface Module

The External Interface module (EIM) handles the interface to devices external to the i.MX21 processor, including generation of chip selects for external peripherals and memory, and provides the following features:

- Six Chip Selects (CS0-5) for external devices, each with 16 Mbyte of address space
- CS0 supports boot from ROM, NAND, or NOR Flash of up to 32 Mbyte of address space
- Programmable protection, port size, and wait states for each chip-select
- Internal/external boot ROM selection
- Selectable bus watchdog counter
- Burst support for external AMD™ or Intel® flash with 32-bit data path
- External Data Transfer Acknowledge (DTACK) support for slower devices connected on CS5

2.4 Bus Master Interface (BMI)

The BMI module enables high speed connection between the i.MX21 processor and the alternate bus master devices in the system. The BMI provides support for the following functions:

- Supports 8- or 16-bit data bus mode
- Supports external bus master read or write to CPU using memory access timing
- Supports CPU write to external bus slave using memory access timing
- Supports ATI graphic chip burst read/write accesses timing

- High communication speed
- Supports DMA

2.5 Inter-Chip Connectivity

This section describes how the modules within the i.MX21 processor interface with each other and provides a high-level overview on how the architecture of the busses are configured and multiplexed.

2.5.1 Inter-IC (I^2C) Bus Module

I^2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I^2C allows additional devices to be connected to the bus for expansion and system development. The I^2C features include:

- Multiple-master operation
- Software-programmable for 1 of 64 different serial clock frequencies
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation and detection
- Repeated START signal generation
- Acknowledge bit generation and detection
- Bus-busy detection

2.5.2 Three Configurable Serial Peripheral Interfaces for High Speed Data Transfer

The i.MX21 processor has three Configurable Serial Peripheral Interface (CSPI) modules that allow rapid data communication with fewer software interrupts than conventional serial communications.

the primary features of the CSPIs include:

- Master/slave configurable (CSPI1 and CSPI2 only)
- Three available chip-selects (CSPI1 and CSPI2) for master mode operation (SS0–SS2)
- Up to 32-bit programmable data transfer
- 8 × 32 FIFO for both transmit and receive data

2.5.3 Two Synchronous Serial Interfaces with Inter-IC Sound (I^2S) and AC97 Host Controller Module (SSI/I^2S/AC97)

Features include the following:

- Supports generic SSI interface for timeslot based communication with synchronous voice codecs

- Timeslot mode supports up to 4 channels for communication among devices Bluetooth voice port, voice codecs and baseband audio ports
- Supports Philips standard Inter-IC Sound (I^2S) bus for external digital audio chip interface at 44.1 kHz and 48 kHz
- AC97 Host Controller mode with support for 2 audio channels supporting variable and fixed rate transfers. Fixed mode only supports 48 kHz sampling rate.
- Used together with the Digital Audio Mux (AUDMUX) module to provide flexible audio and voice routing options

2.6 Peripheral Support

The i.MX21 processor provides a CMOS sensor interface (CSI) that allows the integration of a extensive variety of popular camera features.

2.6.1 CMOS Sensor Interface (CSI)

The CSI features include the following:

- Configurable interface supports wide variety of popular CMOS sensors that output data in YUV, RGB, or Bayer format
- Supports CCIR656 format
- Statistic data generation for auto exposure and auto white balance control which is required for Bayer data
- DMA support for image data transfer
- Private data bus to eMMA Pre-processor module for video and image preprocessing

2.7 Display and Video Modules

There are two separate LCD controllers in the i.MX21 processor—the LCDC and SLCDC that support both dumb and smart LCD panels. A dumb LCD panel has no built-in memory and requires an external controller to send display data at a fixed rate. Such panels typically support high refresh rates suitable for graphics, games, and video applications. The LCD controller in the i.MX21 processor is an AHB master and can transfer display data from system memory (SDRAM).

Smart panels have built-in memory and a display controller. An advantage of the built-in memory and controller, is that the refresh function is done by the local LCD controller and only data that is changing must be updated thus offering a reduced transfer rate and lower power operation.

Both LCD controllers in the i.MX21 processor provide glueless connection to external gray-scale or color LCD panels.

The video input port in the i.MX21 processor supports a direct interface to commonly available CMOS sensors. Together with other system resources (DMA and hardware Pre-processor), viewfinder functions can be achieved with extremely low CPU MIPS and low system power consumption.

2.7.1 LCD Controller (LCDC)

The LCDC features include the following:

- Software programmable screen size (up to 800 × 600) to support single (non-split) monochrome, color STN panels and color TFT panels
- Support color depth for CSTN panels: 4- or 8-bit mapping from 256 × 18 table, 12-bit true color
- Support color depth for TFT panels: 4- or 8-bit mapping from 256 × 18 table, 16-bit/18-bit/24-bit true color
- Up to 16 grey levels out of 16 palettes
- Capable of directly driving popular LCD drivers from manufacturers including Motorola, Sharp, Hitachi, and Toshiba
- Support for data bus width of 16-bit or 18-bit TFT panels
- Support for data bus width of 8-bit, 4-bit, 2-bit, and 1-bit monochrome LCD panels
- Direct interface to Sharp® 320 × 240 and 240 × 320 HR-TFT panels and other generic panels
- Support for logical operation between color hardware cursor and background
- LCD contrast control using 8-bit PWM
- Support for self-refresh LCD modules
- Hardware panning (soft horizontal scrolling)
- Windowing support for one graphic or text overlay

2.7.2 Smart LCD Controller (SLCDC)

The SLCDC transparently and efficiently transfers image data from system memory to an external LCD controller. The SLCDC module contains a DMA controller that transfers image and control data from system memory to the SLCDC FIFO where it is formatted and sent out to the external LCD controller.

The SLCDC can be configured to write image data to an external LCD controller via a 4-line serial, 3-line serial, an 8- or 16-bit parallel interface. The SLCDC has two FIFOs where command and display data are loaded via DMA. The display data is tagged with commands that are used by the SLCDC to communicate display information and data to the Smart LCD panel.

The command tagged data format of the SLCDC provides flexibility and ease of connection to existing and new smart LCD panels.

2.8 enhanced Multimedia Accelerator (eMMA)

The i.MX21 processor comes with an enhanced Multimedia Accelerator (eMMA) comprising an ISO/IEC 14496-2 compliant MPEG-4 encoder and decoder, independent Pre-processing and Post-processing stages which provide exceptional image and video quality. The eMMA represents a major breakthrough to solve the problem of high MIPS requirement for video encode and decode operations in mobile and wireless applications. Tight integration and memory pipelining coupled with AHB master mode operation ensures minimal system loading. To further offload the CPU, live video stream data enters the eMMA module directly through an internal private data interface. The eMMA architecture is shown in Figure 2.

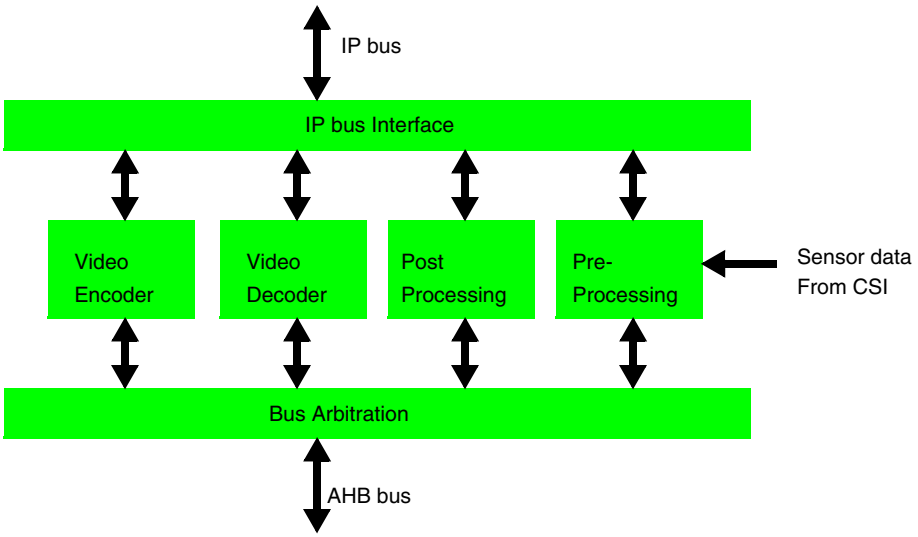

Figure 2. eMMA Architecture

2.8.1 Video Encoder

eMMA provides the following video encoder capabilities:

- Supports MPEG4 and H.263 (Short Video Header)
- Fully conforms to ISO/IEC 14496-2 Visual Simple Profiles Levels 0 to 3
- Supports real-time encoding images of sizes from 32 × 32 up to CIF or QVGA at 30 fps
- Input data format is YUV 4:2:0 (Planar)
- Supports camera stabilization

2.8.2 Video Decoder

eMMA provides the following video decoder capabilities:

- Supports MPEG4 and H.263 (Short Video Header)
- Fully conforms to ISO/IEC 14496-2 Visual Simple Profile Levels 0 to 3
- Supports real-time decoding of image sizes up to CIF or QVGA at 30 fps
- Output data format is YUV 4:2:0 (Planar)

2.8.3 Image Pre-processor (PrP)

The image Pre-processor block, shown in Figure 3, performs color space conversion and image resizing for viewfinder display and data formatting for video encoder and still image for input to a hardware or software based video encoder or image compressor. The Pre-processor has two media input and output paths and can accept input from system memory or from a private data bus connected to the CMOS Sensor Interface (CSI) module. The Pre-processor can apply frame rate control on the live video stream from the CSI module to adjust for different processing load conditions. The Pre-processor's two output channels are used to output RGB data for display of local camera view and to output image data for compression by the hardware encoder or a software encoder (still image or video encode).

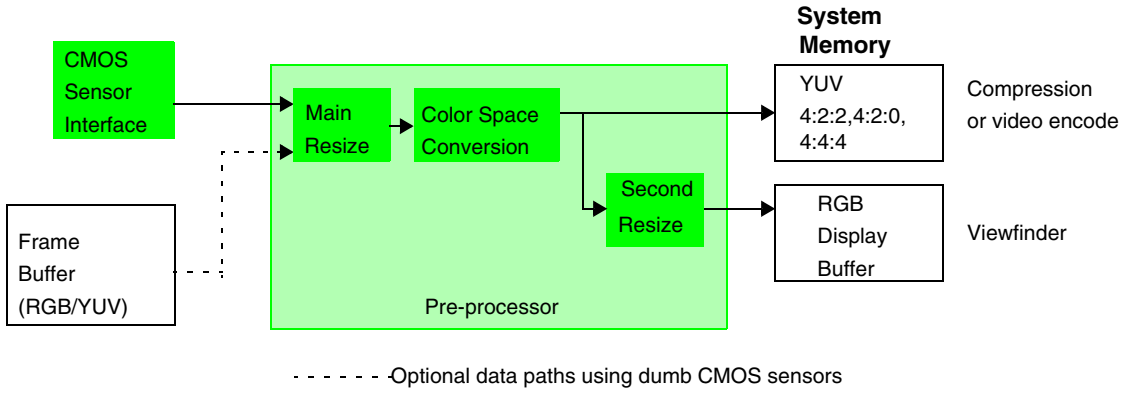

Figure 3. Pre-processor Data Flow

Pre-processor features:

- Data input:
  - System memory
  - Private DMA between CMOS Sensor Interface module and pre-processor
- Data input formats:
  - Arbitrarily unpacked RGB input
  - YUV 4:2:2 (Interleaved)
  - YUV 4:2:0 (Planar)
- Input image size: 2044 × 2044
- Image scaling:
  - Main resize ratio: 8:1–1:1 in integral steps, Horizontal 9:8/vertical 6:5 and Horizontal 9:8/Vertical 1:1
  - Secondary resize ratio for viewfinder: 8:1–1:1 in integral steps
- Output data format:
  - RGB565
  - YUV 4:2:2 (Interleaved)
  - YUV 4:2:0 (Planar)
- RGB data and one YUV data format can be generated concurrently

2.8.4 Postprocessor (PP)

The Postprocessor, shown in Figure 4, performs Deblock, Dering, Image Resize and Color Space Conversion (CSC) functions on the input image data. These functions provide flexibility to meet various RGB formats and YUV formats for display. Besides working in tandem with the decoder sub-block in the eMMA, the Postprocessor can also be used by software decoders (other than MPEG4) to touch up the final output before display. The sub-blocks that perform Deblock, Dering, Resize and CSC operations can be selectively bypassed through software configuration. Figure 4 shows the flow for video postprocessing.

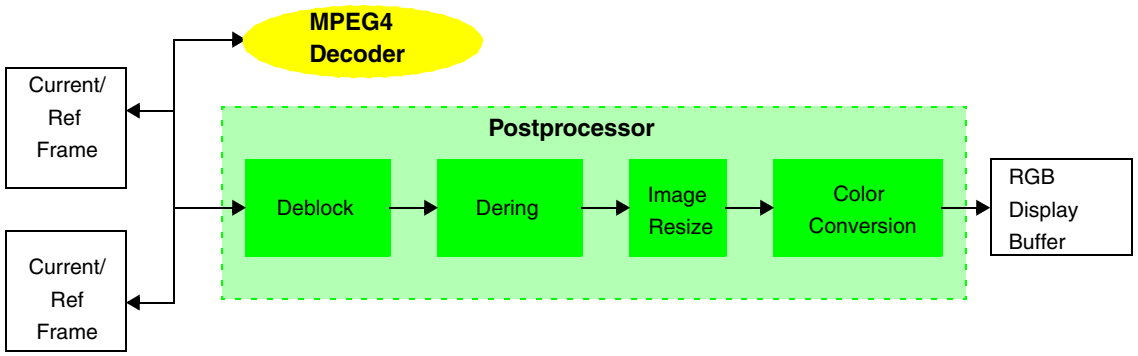

Figure 4. Postprocessor

Postprocessor features:

- Input data:
  - From system memory
- Input format:
  - YUV 4:2:0 (Planar)
- Output format:
  - YUV422
  - RGB444
  - RGB565
  - RGB666
  - RGB888 (unpacked)
- Input Size: Maximum size of 2044 × 2044
- Image Resize:
  - Upscaling ratios ranging from 1:1 to 1:4 in fractional steps
  - Downscaling ratios ranging from 1:1 to 2:1 in fractional steps and a fixed 4:1
  - Ratios provide scaling between QCIF, CIF, QVGA (320 × 240) and QVGA (240 × 320)

2.9 Two Multimedia Card and Secure Digital Host Controller Modules

The Multimedia Card/Secure Digital Host module (MMC/SD) integrates MMC support with SD memory and I/O functions. The features include:

- Fully compatible with the MMC system specification version 2.2
- Fully compatible with the SD Memory Card specification 1.0 and SD I/O specification 1.0 with 1 and 4 channel(s)
- Up to ten MMC cards and one SD supported by standard (maximum data rate with up to ten cards)
- Supports hot swappable operation
- Data rates from 25 Mbps to 100 Mbps
- Dedicated power pin

- Part of the External Memory Interface (EMI) complex comprising the Nand Flash Controller, Wireless External Interface to Memory (WEIM) and SDRAM Controller

2.10 Digital Audio Mux

The Digital Audio Mux (AUDMUX) provides a programmable interconnect fabric for voice, audio and synchronous data routing between the i.MX21 processor's SSI modules and external SSI, audio and voice codecs. The AUDMUX features include:

- Supports 1 host and 3 peripheral interfaces
- Flexible audio, voice and data routing without host processor intervention
- Built-in support for network mode connection of host and peripheral interfaces
- Separate and simultaneous audio paths from hosts to peripherals
- External 4-wire connection to synchronous devices, audio and voice codecs

2.11 Connectivity and Expansion

There are multiple peripheral modules in the i.MX21 processor that provide external connection capability. All peripherals that have FIFOs support DMA transfers to and from the FIFOs. This minimizes CPU intervention and reduces interrupt overhead to the system. The exception to this is the Pulse Width Modulator that includes FIFOs, however, does not support DMA.

2.11.1 Four Universal Asynchronous Receiver/Transmitters (UART1, UART2, UART3, and UART4)

The UART modules are capable of standard RS-232 non-return-to-zero (NRZ) encoding format and IrDA-compatible infrared modes. Each UART provides serial communication capability with external devices through an RS-232 cable or through use of external circuitry that converts infrared signals to electrical signals (for reception) or transforms electrical signals to signals that drive an infrared LED (for transmission) to provide low speed IrDA compatibility to the i.MX21 processor. Features include:

- Supports serial data transmit/receive operation: 7 or 8 data bits, 1 or 2 stop bits, programmable parity (even, odd, or none)
- Programmable baud rates
- Automatic baud rate detection
- 32-bytes FIFO for transmit and 32 half-words FIFO for receive data
- IrDA Serial Infra-Red (SIR) mode support

2.11.2 USB On-The-Go (USB OTG) Controller

The USB controller in the i.MX21 processor implements the USB On-The-Go (USB OTG) supplement. The USB OTG module is complaint to the USB 2.0 and operates at full and low speeds as specified in USB 2.0. The OTG port is capable of connecting to a USB host or client device and uses the Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) to switch between Host and Function roles. One of the dual host ports is dedicated for connection to a smartphone USB client device and the other host port

is available for connection to other client devices. The connection to the smartphone forms the interprocessor link as an alternate to a UART-based link.

Built-in switching logic implements a bypass mode in which the internal host port is bypassed to allow an external USB host and the smartphone USB client to be directly connected. This feature enables the external USB host to directly control the smartphone modem for debug or for production programming. Figure 5 shows the USB OTG block.

The USB OTG module is a bus master and takes ownership of the bus for DMA. This allows the USB OTG to continue operation while the CPU is in a low power mode.

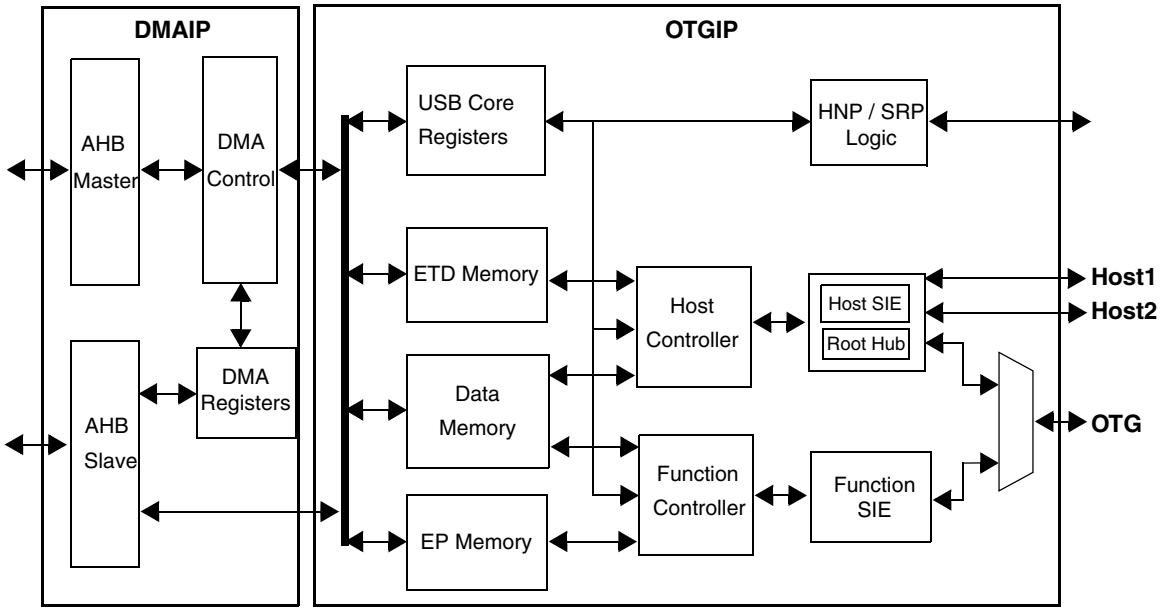

Figure 5. USB On-The-Go Controller Block Diagram

- Compliant with the USB 2.0 specification for operation at full speed (12 Mbit/sec) and low speed (1.5 Mbit/sec)
- Fully compliant with the USB On-The-Go specification
- Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) implemented in hardware and can also be controlled by software
- Transaction scheduling and transfer level protocol implemented in hardware including bandwidth management, data toggle and retry
- AMBA AHB 2.0 Bus Master DMA Controller:
  - 32 DMA Channels for Host Controller EndPoint Transfer Descriptors
  - 32 DMA Channels for Function Controller EndPoint Descriptors
- USB function supports 32 physical endpoints:
  - 16 IN endpoints and 16 OUT endpoints
  - Programmable for type (control, interrupt, bulk, isochronous), packet size, and buffering
- Double buffering support for all four types of Host and Function controller transactions

- Separate descriptor and data memory space
- Direct device-to-device transfers in one frame
- Power savings mode for Host Controller and suspend mode for Function Controller
- The USB Host port 1 supports external transceiver bypass mode

2.12 Debug Capability

The i.MX21 processor offers designers and programers with full-debug capabilities through industry-standard JTAG interface and the ability to bootload using either a serial or USB interface.

- UART Bootstrap mode function:
  - Allows system initialization and program or data download to system memory via USB or UART1
  - Accepts execution command to run program stored in system memory
  - Supports memory/register read/write operation of selectable data size of byte, half-word, or word
  - Provides a 16-byte instruction buffer for ARM instruction storage and execution
- USB Bootstrap mode function
  - Supports bootstrapping through USB OTG port
- JTAG port to support generic ARM debug tools

2.12.1 PCMCIA/CF Interface

The PCMCIA/CF host controller module provides all the control logic for a PCMCIA socket interface and requires only additional external analog power switching logic and buffering. The controller supports one PCMCIA socket and includes the following features:

- PCMCIA/CF host controller interface compliant with the PCMCIA standard release 2.1 (for I/O Cards) and fully compliant with the Compact Flash Specification V1.4
- Supports one PCMCIA or CF socket
- Supports hot-insertion, card detection and removal
- Mapping to common memory space, attribute memory space and I/O space.
- Supports 5 programmable memory and IO windows.
- Generates a single interrupt to the CPU
- Programmable card access timing to interface with slower devices
- Supports TrueIDE mode
- Provides special control signals for external buffering to separate high and low speed paths

2.12.2 Keypad Port

The Keypad Port is a 16-bit peripheral which can be used either for keypad matrix scanning or as general purpose I/O. Features include:

- Supports up to 8 × 8 external key pad matrix

- Open drain design
- Glitch suppression circuit prevents erroneous key detection
- Multiple keys detection
- Standby key press detection

2.12.3 Fast Infra-Red Interface (FIRI)

The Fast Infra-Red Interface (USB device module) in the i.MX21 processor implements both the Medium Infra-Red (MIR) and Fast Infra-Red (FIR) protocols. In MIR mode, the FIRI supports wireless communications at 0.576 Mbps and 1.152 Mbps and uses a framed transmission protocol which follows the High-Level Data Link Controller (HDLC) protocol. In FIR mode, the module operates at 4 Mbps with 4 Pulse Position Modulation (4PPM) defined by IrDA, version 1.4.

In addition to the MIR and FIR modes, the i.MX21 processor supports SIR protocol on all of the UART modules. Only UART1 may be used together with the FIRI as these two modules share their pins for transparent speed and protocol stepping from SIR to MIR or SIR to FIR modes.

Figure 6 shows the FIRI sharing pins with the UART module and pin selection is controlled via GPIO configuration.

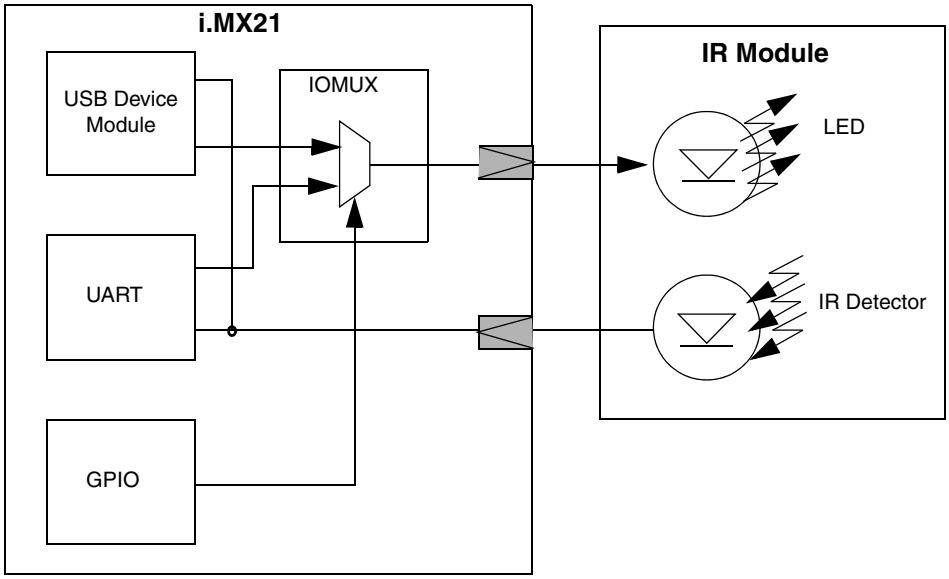

Figure 6. Fast Infra-Red Interface

The USB device module can be divided to the following functional parts:

- Packet assembler
- Searcher
- 4PPM modulator/demodulator
- CRC32 encoder and decoder
- DMA capable receive and transmit FIFOs

2.12.4 1-Wire® Interface

The 1-Wire module is a peripheral device that communicates with the ARM926EJ-S Core and provides a communication line to a 1 Kbit Add-Only Memory (DS2502). The 1-Wire interface features include:

- Supports 1-Wire interface to a 1Kbit Add-Only Memory (DS2502)
- Implements 1-Wire protocol defined by Dallas Semiconductors

2.13 Power Management

The i.MX21 processor's power management features are as follows:

- Support for 3 power modes of operation: RUN, DOZE, and STOP
- Aggressive clock gating within modules to minimize CMOS switching power
- Active well biasing technique to reduce standby mode current consumption

2.14 Electronic and Package Information

The i.MX21 processor features the following electronic and package information:

- Operating voltage
  - I/O voltage: 1.7 V to 3.3 V
  - Internal logic voltage: 1.45 V to 1.65 V
- Package
  - Type: 0.65 mm and 0.8 mm pitch MAPBGA
  - Dimensions: 14mm × 14mm and 17mm × 17mm
  - Pins: 289

3 Document Revision History

This revision, Rev. 2.1, contains the changes identified in Table 1.

Table 1. Document Revision History

Location	Description of Change
Section 2.1, "ARM926EJ-S Core Complex" Core features	Removed references to the ARM926EJ-S ROM Patch module.
Section 2.5.2, "Three Configurable Serial Peripheral Interfaces for High Speed Data Transfer	• Clarified master/slave functionality of the CSPIs
Section 2.5.3, "Two Synchronous Serial Interfaces with Inter-IC Sound (I2S) and AC97 Host Controller Module (SSI/I2S/AC97)	• Added reference to AC97 only supporting 48 kHz sample rate.
Section 2.2, "System Control and Timers	Removed reference to Security.
Section 2.7.1, "LCD Controller (LCDC)	Changed first bullet from "...(up to 640x480)..." to "...(up to 800x600)..."
Section 2.11.2, "USB On-The-Go (USB OTG) Controller	Clarification of first two paragraphs.

NOTES

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

***For Literature Requests Only*:**
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-521-6274 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: MC9328MX21P
Rev. 2.1
07/2007

freescale™
semiconductor